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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/732,240	12/07/2000	Thomas George Ference	BUR919990304US1	9501

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Kevin P. Radigan, Esq.
HESLIN & ROTHENBERG, P.C.
5 Columbia Circle
Albany, NY 12203

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/732,240	FERENCE ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 7, 10 - 14 and 30 - 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 7, 10 - 14 and 30 - 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal Brief

1. In view of the appeal brief filed on January 12, 2004, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 30, 34 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Downes '277.

Regarding claim 1, Downes discloses in e.g., Fig. 1, Figs. 4, column 7, lines 38 - 49 and column 8, lines 10 - 31 a structure comprising:

- a first substrate (10) and a second substrate (20); and
- first solder bumps (14) and second solder bumps (16) offset therebetween,
- wherein said first solder bumps and said second solder bumps are separate solder bumps disposed between said first substrate and said second substrate; and
- wherein said second solder bumps have at least a portion that melts at a lower temperature than said first solder bumps; and

The limitation -- "wherein the second solder bumps are for aligning the first substrate and the second substrate before melting the first solder bumps." -- sets forth an intended use of the invention, but does not require that the first solder bumps actually be melted. The low-temperature bumps (16) of Downes inherently aligns the substrates upon reflow. See e.g., page 10, second paragraph of Applicant's specification acknowledging that the reflow process inherently causes alignment.

Regarding claim 30, Downes discloses in e.g., Fig. 1, Figs. 4, column 7, lines 38 - 49 and column 8, lines 10 - 31 a structure comprising:

- a first substrate (10) having a main surface with first solder bumps (14) and second solder bumps (16) separately disposed thereacross; and
- wherein the second solder bumps have at least a portion that melts at a lower temperature than the first solder bumps,

- the second solder bumps being for aligning (inherent function of any solder bumps) the first substrate (10) to a second substrate (20) before melting the first solder bumps.

Regarding claims 34 and 35, Downes discloses in e.g., Fig. 1, Figs. 4, column 7, lines 38 - 49 and column 8, lines 10 - 31 the second solder bumps (16) having a uniform composition and melting at a lower temperature than the first solder bumps (14).

4. Claims 1 – 3, 5 - 7, 10, 11 and 30 – 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Ito et al. '700.

Regarding claim 1, Ito et al. discloses in e.g., Fig. 3, column 6, lines 15 - 22 and column 8, lines 34 - 35 a structure comprising:

- a first substrate (1) and a second substrate (B); and
- first solder bumps (10; copper) and second solder bumps (24; a tin-lead alloy) offset therebetween,
- wherein said first solder bumps and said second solder bumps are separate solder bumps disposed between said first substrate and said second substrate; and
- wherein said second solder bumps have at least a portion that melts at a lower temperature than said first solder bumps; and
- wherein the second solder bumps are for aligning (inherent function of any solder bumps) the first substrate and the second substrate before melting the first solder bumps.

Regarding claims 2 and 31, Ito et al. discloses in e.g., Fig. 3 the second solder bumps (24) being larger than the first solder bumps.

Regarding claim 3, Ito et al. discloses in e.g., Fig. 3 disclose the second solder bumps (24; a tin-lead alloy) comprising a portion having a higher concentration of tin than does the first solder bumps (10; copper).

Regarding claim 5, Ito et al. discloses in e.g., Fig. 3 the portion (any part in the second solder bumps; at the top portion of the second solder bump) being adjacent to the second substrate.

Regarding claim 6, Ito et al. discloses in e.g., Fig. 3 the portion (any part in the second solder bumps; top and central portion of the second solder bumps) being centrally located within the second solder bump.

Regarding claim 7, Ito et al. discloses in e.g., Fig. 3 the portion being the entire second solder bumps.

Regarding claims 10 and 32, Ito et al. discloses in e.g., Fig. 3, column 6, lines 15 - 22 and column 8, lines 34 – 35 the second solder bumps (24; a tin-lead alloy, melting point < 327 °C) melting at a temperature at least 25 °C less than the first solder bumps (10; copper, melting point 1083 °C).

Regarding claims 11 and 33, Ito et al. discloses in e.g., Fig. 3 the first substrate (elements 1 and 5) comprising a first semiconductor chip (5).

Regarding claim 30, Ito et al. discloses in e.g., Fig. 3, column 6, lines 15 - 22 and column 8, lines 34 - 35 a structure comprising:

- a first substrate (1) having a main surface with first solder bumps (10; copper) and second solder bumps (24; a tin-lead alloy) separately disposed thereacross; and
- wherein the second solder bumps have at least a portion that melts at a lower temperature than the first solder bumps,
- the second solder bumps being for aligning (inherent function of any solder bumps) the first substrate (1) to a second substrate (B) before melting the first solder bumps.

Regarding claims 34 and 35, Ito et al. discloses in e.g., Fig. 3, column 6, lines 15 - 22 and column 8, lines 34 – 35 the second solder bumps (24; a tin-lead alloy) having a uniform composition and melting at a lower temperature than the first solder bumps (10; copper).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. in view of Behun et al. '844.

Ito et al. discloses the claimed invention except for the portion comprising an eutectic concentration of tin. However, Behun et al. teaches in e.g., Fig. 3 and column 4, lines 14 – 23 solder balls (18, high melting point) with a portion (16 and 13, low melting

point) comprising an eutectic concentration of tin (see column 4, lines 6 - 10). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ito et al. by using the solder balls that further comprise an eutectic portion as taught by Behun et al. The ordinary artisan would have been motivated to further modify Ito et al. in the manner described above for at least the purpose of (1) increasing attachment between the high melting point solder balls to the pad of the package and (2) providing more readily testable and reliability for the package (column 2, lines 66 – 68).

7. Claims 12 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. in view of Bertin et al. '640.

Ito et al. discloses the claimed invention except for the second substrate comprising a second semiconductor chip (claim 12), the second chip being larger than the first chip (claim 13), and the second chip further comprising wire bond pads for bonding to a printed circuit board (claim 14). However, Bertin et al. teaches in e.g., Fig. 5, column 1, lines 40 – 43 and column 2, lines 61 – 65 a second substrate (30 in Fig. 4) comprising a second semiconductor chip (30), the second chip (30) being larger than a first chip (40), and the second chip (30) further comprising wire bond pads (pads that are connected at the end of the wire 28) for bonding to a printed circuit board (72). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Ito et al. by using the second chip to be the second substrate, size of the second chip to be bigger than the first chip and the wire bond pads as taught by Bertin et al. The ordinary artisan would have been motivated to further modify Ito et al. in the manner

described above for at least the purpose of reducing the size and increasing the functionality of semiconductor devices formed according to Ito et al.

Response to Arguments

8. Applicant's arguments, see page 6 – 10 of the Appeal Brief, filed January 12, 2004, with respect to the rejection(s)of claim(s) 1 – 7, 10 – 14 and 30 – 35 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art references.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ho '036 discloses two different groups of solder bumps, each one of the groups has a different melting points.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

c.c.
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BRADLEY BAUMEISTER
L. PRIMARY EXAMINER
PRIMARY EXAMINER